UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,667	08/22/2003	Naresh Thapar	IR-2326 (2-3640)	1010

2352 7590 08/05/2004

OSTROLENK FABER GERB & SOFFEN
1180 AVENUE OF THE AMERICAS
NEW YORK, NY 100368403

EXAMINER	
PRENTY, MARK V	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 08/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/646,667	THAPAR, NARESH	
	Examiner	Art Unit	
	MARK V PRENTY	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7,8,15 and 19* is/are rejected.

7)☒ Claim(s) *3-6,9-14,16,17,20 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This Office Action is in response to the papers filed on August 22, 2003.

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-17 and 19-21, drawn to a semiconductor device, classified in class 257, subclass 330.

II. Claim 18, drawn to a method of making a semiconductor device, classified in class 438, subclass 197.

The inventions are distinct, each from the other because:

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another and materially different process, such as by doping the trenched polysilicon gates in situ.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

On August 2, 2004, Kourosh Salehi (Reg. No. 43,898) telephonically elected without traverse to prosecute the invention of Group I, claims 1-17 and 19-21. Affirmation of this election must be made by applicant in replying to this Office action.

Claim 18 is withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Dependent claims 2, 5 and 6 are objected to because "said one of the contact types" should read, "said one of the conductivity types."

Independent claim 19 is objected to because "the tops of said mesas having a central Schottky barrier-receiving trench of relatively high resistivity surface flanked by source regions of relatively high resistivity surface," should read, "the tops of said mesas having a central Schottky barrier-receiving trench of relatively high resistivity surface flanked by source regions of relatively low resistivity surface" (see the specification at paragraph [0023], for example).

Claims 20 and 21 depend on independent claim 19 and are thus similarly objected to.

Claims 1, 2, 7, 8, 15 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Baliga et al. (United States Patent 5,679,966 – hereafter Baliga).

With respect to independent claim 1, Baliga discloses a MOSgated accumulation channel field effect transistor (see the entire patent, including the Fig. 11 disclosure) comprising a highly conductive silicon (note column 7, lines 43-45) substrate 26A of one of the conductivity types; a drift region 26B of said one of the conductivity types disposed above said substrate; a channel region 26C of said one of the conductivity types disposed above said drift region and having an impurity concentration less than that of said substrate; a plurality of trenches 25 extending through said channel regions

and into said drift region; each of said trenches having respective gate oxide liners along their vertical walls, and insulation liners at the bottoms of said trenches; a gate 30 of the other conductivity type (see column 8, lines 35-40) filling the interior of each of said trenches; an insulation cap over the tops of each of said gates in each of said trenches; a highly conductive source region 28 disposed at the tops of the mesas between each of said trenches and above said channel regions which are in the mesas between each of said trenches; a Schottky barrier contact area 27 formed in the top of each of said mesas; and a top contact metal 22 connected to both said source regions and to said Schottky barrier contacts areas.

Claim 1 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Baliga.

With respect to dependent claim 2, Baliga's said one of the conductivity types is the N type.

Claim 2 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Baliga.

With respect to dependent claims 7 and 8, Baliga's transistor includes a second plurality of trenches formed in at least selected ones of said mesas and spaced from the walls of said trenches forming said mesas; said Schottky barrier contact areas 27 being formed in respective ones of said second plurality of trenches.

Claims 7 and 8 are thus rejected under 35 U.S.C. 102(b) as being anticipated by Baliga.

With respect to dependent claim 15, Baliga's gates 30 are formed of P type polysilicon (see column 8, lines 35-40).

Claim 15 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Baliga.

With respect to independent claim 19, Baliga discloses a MOSgated accumulation channel field effect transistor (see the entire patent, including the Fig. 11 disclosure) having a plurality of mesas separated by parallel gate-filled trenches 25; the tops of said mesas having a central Schottky barrier-receiving trench of relatively high resistivity surface flanked by source regions 28 of relatively [low] resistivity surface; and a top contact 22 connected to said source region surface with an ohmic contact and to said Schottky barrier receiving trench surface with a Schottky contact 27.

Claim 19 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Baliga.

Claims 3-6, 9-14, 16, 17, 20 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable over the prior art of record if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record does not disclose or suggest the allowable MOSgated accumulation channel field effect transistor taken as a whole, including the Schottky barrier contact.

Thapar (United States Patent 6,580,123) and Thapar (United States Patent Application Publication 2004/0119103) are related to this application.

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.

Mark Prenty

Mark V. Prenty
Primary Examiner